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Operational amplifier with constant offset and apparatus comprising such an operational amplifier

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DESCRIPTION

Operational amplifier with constant offset and apparatus comprising such an operational amplifier

Field of the invention

The present invention concerns operational amplifiers and systems, such as LCD source drivers, based thereon.

Background of the invention

The liquid crystals (LC) of a liquid crystal display (LCD) are typically driven with an alternating driving voltage, referred to as LC voltage, whose peak to peak voltage is defined by a transmission-voltage curve 10, as depicted in Fig. 1. In this Figure, the transmittance vs. the LC voltage is depicted. The alternating LC voltage is used to avoid degeneration of the LCs. In order to obtain a desired grey level, the distance between the respective positive voltage peak 11 and the negative voltage peak 12 is to be kept at a constant voltage level referred to as VCOM. In Fig. 1, the voltages applied on the LC are represented by the two arrows 11 and 12, the first arrow 11 pointing in the positive LC voltage direction and the second arrow 12 pointing in the negative LC voltage direction.

The LC voltage across the LC is subject to two different errors:

- differential errors which may give as a result visible dim lines,
- common mode errors, which usually result in flickering.

Fig. 2 shows the worst cases of four “pairs” of LC voltages that can occur in the source driver of an LCD, for a given offset. The output N has a positive differential error of 2*offset since both peaks 13 and 14 reach the respective maximum offset 17, and the output N+1 has a negative differential error of -2*offset since both peaks 15 and 16 reach the respective minimum offset 18. The total differential error between two adjacent LC lines N and N+1, if the first line N is driven with Y_N and the second line N+1 is driven with Y_{N+1} is:

$$Y_{N_DIFF_ERR} - Y_{N+1_DIFF_ERR} = 4 * \text{offset} \quad (1)$$

For these two outputs Y_N and Y_{N+1} the common voltage error is 0, because the average of the driving voltages 13 through 16 is equal to V_{COM} .

The outputs $N+2$ and $N+3$ do not have any differential error. The difference of the driving voltages 21, 22 applied on the LC is equal to the difference of the two target voltages, they have, however, a common voltage error 25. The difference of the driving voltages 23, 24 is equal to the difference of the two target voltages, they have, however, a common voltage error 26. The output $N+2$ has a positive common error 25 of offset, and the output $N+3$ has a negative differential error 26 of – offset. The difference of the two common voltage errors 25 and 26 is:

$$Y_{N_COMM_ERR} - Y_{N+1_COMM_ERR} = 2 * \text{offset} \quad (2)$$

For a given offset the maximum differential error voltage is twice the maximum common mode error.

The LC are far more sensible to differential voltages than to common mode voltages, so there is a need for a driving system that allows to provide precise differential LC voltages.

Liquid Crystals (LC) need to be driven with an alternate LC voltage, as explained above, that should have a low differential mode error. A very simple method to reduce differential mode errors is to drive the LC on both P and N sides with the same buffer. In an ideal case the buffer will have an offset, but this will be more or less constant along the output range. The voltage drop ΔV across the LC would be:

$$\Delta V = V_{\gamma P} + V_{Offset} - (V_{\gamma N} + V_{Offset}) = V_{\gamma P} - V_{\gamma N} \quad (3)$$

As one can derive from equation (3), one loses the dependence on the buffer offset, since the term $+V_{Offset} - V_{Offset}$ is equal to zero. This strategy has been implemented on 6bit drivers with rail-to-rail operational amplifiers. The drawback of this approach is that close to the rails one of two input doublets of the source driver's input stage switches off, with the result of an even big differential error. On a 6bit driver, the bit widths close to the rail are quite big. If the extra error does not exceed 1/3 of the bit width, on the LCD screen no visible effect will be seen.

The situation changes drastically with an 8bit device. The bit width, in any part of the gamma curve (see Fig. 1), will be 4 times smaller. The precision of a traditional rail-to-rail operational amplifier is not enough for such an 8bit device.

A standard rail-to-rail amplifier 30 is depicted in Fig. 3. This Figure shows a common rail-to-rail input stage 30, composed by two transistor doublets. The first transistor doublet comprises two PMOS transistors M3, M4, and the second transistor doublet comprises two NMOS transistors M1, M2. The input stage 31 has a differential input with negative and positive input terminals 32, 33. The outputs of the two transistor doublets are connected to the second stage 34 of the rail-to-rail amplifier 30. On the right hand side of Fig. 3, the dynamic range of the two transistor doublets is illustrated. As one can see, only in the middle range 35 both transistor doublets are operable. The saturation voltage V_{sat} indicated is the voltage drop needed by a current supply to work properly. $V_{gs,NMOS}$ and $V_{gs,PMOS}$ are the gate source voltages of the NMOS and PMOS transistors.

The total offset present in the rail-to-rail amplifier 30, when all the devices are operable, is:

$$V_{off,TOT} = V_{off,P} + V_{off,N} + \frac{1}{2}K \quad (4)$$

Where K is the offset contribution of the second stage 34 when one of the two transistor doublets is switched off. $Gm_{1ST_STAGE} = Gm_{NMOS} + Gm_{PMOS}$ and $Gm_{NMOS} = Gm_{PMOS}$ is also considered in this equation (4). In this equation and in subsequent equations, the suffix N or NMOS refers to the NMOS transistors and the suffix P or PMOS refers to the PMOS transistors.

If one of the complementary transistor doublets of the input stage 31 switches off, the contribution to the offset of the 2nd stage 34 doubles, because the input transconductance Gm_{1ST_STAGE} halves. When one of the transistor doublets of the input stage 31 switches off and the $Gm_{NMOS} \neq Gm_{PMOS}$, if the offset contribution of the second stage 34 when the PMOS transistors M1, M2 switch off is K, when the NMOS transistors M3, M4 switch off, the total offset is:

$$V_{off,TOT} = V_{off,P} + K \frac{Gm_N}{Gm_P} \quad (5)$$

One now can calculate the maximum differential error Δ_{err} :

$$\Delta_{\text{err}} = V_{\text{off}_P} + K \frac{Gm_N}{Gm_P} - (V_{\text{off}_N} + K) = V_{\text{off}_P} - V_{\text{off}_N} + K \left(\frac{Gm_N}{Gm_P} - 1 \right) \quad (6)$$

When both input MOS transistors work, the differential error is 0 if: $Gm_N = Gm_P$, $V_{\text{off}_N} = V_{\text{off}_P}$. It is maximum when $V_{\text{off}_{NMOS}} = -V_{\text{off}_{PMOS}}$, $Gm_N \neq Gm_P$, and it is:

$$\Delta_{\text{err}_{\text{MAX}}} = 2V_{\text{off}_P} + K \left| \frac{Gm_N}{Gm_P} - 1 \right| \quad (7)$$

Prior art source drivers, as the one described in connection with Fig. 3, are not designed to provided the required precise differential LC voltages. Conventional amplifiers used in source drivers, for instance, do not provide for a constant offset over the whole input range.

It is thus an objective of the present invention to improve amplifiers so that they have a constant offset over the whole input range.

It is another objective of the present invention to provide an amplifier that is better suited for being used in liquid crystal displays than conventional amplifiers.

In particular, the present invention is directed to an LCD source driver that substantially obviates the problems due to limitations and disadvantages of the related art.

SUMMARY OF THE INVENTION

These disadvantages of known systems, as described above, are reduced or removed with the invention as described and claimed herein.

An apparatus in accordance with the present invention is claimed in claim 1.

Various advantageous embodiments are claimed in claims 2 through 9.

Another apparatus in accordance with the present invention is claimed in claim 10.

Various advantageous apparatus are claimed in claims 11 through 13.

Additional features and advantages of the invention will be set forth in the description that follows, and in part will be apparent from the description.

Brief description of the drawings

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

- FIG. 1** shows a typical Transmission Voltage Curve, as used in LCD displays;
- FIG. 2** shows the four driving voltages worst cases that can be present in a Source Driver of an LCD display;
- FIG. 3** is a block diagram of a conventional rail-to-rail input stage, as used in LCD displays;
- FIG. 4** is a block diagram of a conventional LCD display;
- FIG. 5A** is a schematic block diagram of a rail-to-rail input stage, according to the present invention, where a PMOS transistor doublet is used;
- FIG. 5B** is a schematic block diagram of a rail-to-rail input stage, according to the present invention, where an NMOS transistor doublet is used;
- FIG. 6** is a schematic block diagram of another embodiment, according to the present invention;
- FIG. 7** is a schematic block diagram of the embodiment illustrated in Fig. 6;
- FIG. 8** is a schematic block diagram of a part of a source driver, according to the present invention;
- FIG. 9** is a schematic block diagram of a control signal generator, according to the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Before addressing detailed embodiments of the present invention, the typical block diagram of an LCD system is addressed.

Fig. 4 shows a typical block diagram of an LCD system. Low Voltage Differential Signaling (LVDS) is used as the interface between a host computer (not illustrated in Fig. 4) and a panel module 40. An LVDS receiver function 41 is typically integrated into a panel timing controller 42. A reduced swing differential signaling (RSDS) bus 43 is located between the panel timing controller 42 (TCON) serving as transmitting circuit and a source driver bank 44 serving as receiving circuit. RSDS is a trademark of National Semiconductor Corporation. The RSDS bus 43 is typically a differential bus that is eight pairs wide plus a clock pair and it may have a multidrop bus configuration. The source driver bank 44 comprises a plurality of RSDS source drivers 44.1. Typically, each source driver 44.1 of the source driver bank 44 serves n column electrodes (with n = 384 or 480, for example) of the display panel 46 by providing analog output signals. In the present example, each source driver 44.1 serves n=4 column electrodes only. There is a gate driver array 45 comprising an array of gate drivers 45.1. Several of the rows of the panel 46 are driven by any of these gate drivers 45.1. The gate drivers 45.1 are activated sequentially to turn on one row of pixels at a time, allowing analog voltages driven onto the columns to be applied to each row of pixels in series. The panel 46 may be a TFT-LCD panel with 640 pixels width and 480 lines (or rows) of pixels, for example. The source drivers 44.1 have interfaces using a differential clock signal (CLK+ and CLK-) received via the RSDS bus 43 to strobe the video data.

A TFT-LCD source driver 44.1 is a circuit that supplies LC voltages to LCD pixel columns. The function of a TFT-LCD source driver 44.1 is explained referring to Fig. 4. Digital video signals are inputted to the TFT-LCD source driver 44.1. In an active matrix type liquid crystal display panel 46 constituting a display apparatus 40, source lines O1 to ON and gate lines L1 to LM are formed in an NxM matrix. At each intersection of the lines, a thin film transistor is disposed. The thin film transistors are not shown in Fig. 4. Voltages at the source lines O1 to ON are selectively supplied to pixel electrodes P via the thin film transistors. A gate driver 45.1 formed by a semiconductor integrated circuit delivers gate signals to the gate lines L1 to LM. In a horizontal scanning period, the source drivers 44.1 supply an alternating LC voltage (also referred to as

reference voltage), which is generated in accordance with video data received via the differential bus 43. In other words, a source driver is a circuit that supplies video signals to an LCD pixel array.

According to the present invention, circuits are provided that have a constant offset over the whole range of the differential input signal.

In the following sections, an operational amplifier is addressed which has a rail-to-rail input stage and, in accordance with the present invention, a constant offset on the whole input range. The input stage comprises two transistor doublets, as in prior art systems. According to the present invention, for a given input signal only the transistor doublet needed is used. If one has an input signal close to ground, one uses only a PMOS transistor doublet and if one has an input signal close to the supply voltage VCC, one uses only an NMOS transistor doublet. According to the present invention, the unused (idle) transistor doublet is maintained in an active state. The purpose of this is to keep its transconductance (G_m) of the idle transistor doublet always constant and equal in value to the transconductance of the used transistor doublet. For a source driver, a possible solution in accordance with the present invention, is the following: for positive gamma data the NMOS transistor doublet is used and for negative gamma the PMOS transistor doublet is used. Using the input stage in this way, the offset stays constant only if the transconductance of the NMOS transistor doublet and the PMOS transistor doublet are the same, that is $G_{m_{NMOS}} = G_{m_{PMOS}}$.

Figures 5A and 5B illustrate how to obtain a constant offset with a rail-to-rail input stage 50.

In accordance with CMOS technology, the apparatus comprises a plurality of MOS transistors of both the NMOS and PMOS type. In the drawings and in the description, the NMOS transistors are designated with the prefix N and the PMOS transistors are designated with the prefix P.

A first apparatus in accordance with the present invention is depicted in Figures 5A and 5B. In these Figures, an input stage 50 of a source driver is depicted. The input stage 50 comprises an NMOS transistor doublet N1, N2 with a first differential input 52.1, 53.1 for receiving analog input signals In+, In-. The input stage 50 furthermore comprises a PMOS transistor doublet P3, P4 with a second differential input 52.2, 53.2 for receiving input signals In+, In-. In order to be

able to direct the input signals In+, In- either to the first transistor doublet N1, N2 or to the second doublet P3, P4, switching means are employed that selectively direct the analog input signal In+, In- either to the first differential input 52.1, 53.1 or to the second differential input 52.2, 53.2. The switching function is controlled by a switching signal, preferably a digital switching signal. For sake of simplicity, the switching means are not depicted in Figures 5A and 5B. More details about the switching means will be given in connection with Fig. 6.

Fig. 5A shows a situation where the differential input signal In+, In- is directed to the PMOS transistor doublet P3, P4 and Fig. 5B shows a situation where the differential input signal In+, In- is directed to the NMOS transistor doublet N1, N2. The drains 55.1 through 55.4 of the four transistors N1, N2, P3, P4 are connected to a second stage 54. The second stage 54 typically comprises an amplifier. In order to ensure that the transconductance Gm_{NMOS} of the NMOS transistor doublet and the transconductance Gm_{PMOS} of the PMOS transistor doublet are the same, no matter whether positive gamma data or negative gamma are applied to the differential inputs 52.1, 52.2, 53.1, 53.2, the idle transistor doublet, i.e. the one transistor doublet not being used, is kept active. In other words, while the first transistor doublet processes the input signal, the other transistor doublet's transconductance Gm is kept constant.

The precision of any amplifier using the invention depends on how well the Gm_{NMOS} and Gm_{PMOS} of the transistor doublets N1, N2 and P3, P4 are matched. In the following it is described which parameters can influence the Gm precision during the process diffusion. The Gm can be calculated with the following formula:

$$Gm = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (8)$$

The ratio between the two Gm is:

$$\frac{Gm_{PMOS}}{Gm_{NMOS}} = \frac{\sqrt{2\mu_p C_{ox} \frac{W_p}{L_p} I_D}}{\sqrt{2\mu_n C_{ox} \frac{W_n}{L_n} I_D}} = \frac{\sqrt{\mu_p} \frac{W_p}{L_p}}{\sqrt{\mu_n} \frac{W_n}{L_n}} = \frac{\sqrt{\mu_p}}{\sqrt{\mu_n}} \frac{\sqrt{\frac{W_p}{L_p}}}{\sqrt{\frac{W_n}{L_n}}} \quad (10)$$

C_{ox} and I_D are the same. If one supposes for the sake of simplicity that the geometric errors on W and L of the transistors are small (usually the input transistors are quite large), the main source of error is the process spread on the mobility of the NMOS and PMOS transistors, that are more or less independent from each other.

The mobility can change +/-15% with respect to the typical value. Hence the previous ratio will be:

$$0.86 = \sqrt{\frac{0.85}{1.15}} \leq \frac{Gm_{PMOS}}{Gm_{NMOS}} \leq \sqrt{\frac{1.15}{0.85}} = 1.16 \quad (11)$$

In case the Gm is not identical, the offset does not stay constant. One can calculate how big the contributions of the first stage 51 and the second stage 54 are. One can start calculating the contribution to the offset of the first stage 51. For a positive gamma curve, the offset will be:

$$V_{off_{1ST_P}} = V_{off_N} + V_{off_P} \frac{Gm_{PMOS}}{Gm_{NMOS}} \quad (12)$$

For a negative gamma curve, the offset will be:

$$V_{off_{1ST_N}} = V_{off_P} + V_{off_N} \frac{Gm_{NMOS}}{Gm_{PMOS}} \quad (13)$$

The contribution to the offset of the second stage 54, if for a positive gamma curve is $V_{off_{2ND_P}}=K$, for the negative gamma curve is:

$$V_{off_{2ND_N}} = K \frac{Gm_{PMOS}}{Gm_{NMOS}} \quad (14)$$

The differential error is the difference between the offset when a value of the positive gamma curve is driven, and the offset when a value of the negative gamma curve is driven:

$$\Delta_{err} = V_{off_{1ST_N}} + V_{off_{2ND_N}} - (V_{off_{1ST_P}} + V_{off_{2ND_P}}) \quad (15)$$

If one inserts in this expression (15) what was calculated before in equation (14), one obtains:

$$\Delta_{\text{err}} = V_{\text{offP}} \left(1 - \frac{Gm_{\text{PMOS}}}{Gm_{\text{NMOS}}} \right) + V_{\text{offN}} \left(\frac{Gm_{\text{NMOS}}}{Gm_{\text{PMOS}}} - 1 \right) + K \left(\frac{Gm_{\text{PMOS}}}{Gm_{\text{NMOS}}} - 1 \right) \quad (16)$$

If $\left| \frac{Gm_{\text{NMOS}}}{Gm_{\text{PMOS}}} - 1 \right| \ll 1$, then $\left| \frac{Gm_{\text{NMOS}}}{Gm_{\text{PMOS}}} - 1 \right| \approx \left| 1 - \frac{Gm_{\text{PMOS}}}{Gm_{\text{NMOS}}} \right|$, so the previous equation (16)

becomes:

$$\Delta_{\text{err}} = \left| 1 - \frac{Gm_{\text{PMOS}}}{Gm_{\text{NMOS}}} \right| (V_{\text{offP}} + V_{\text{offN}} + K) = \left| 1 - \frac{Gm_{\text{PMOS}}}{Gm_{\text{NMOS}}} \right| V_{\text{offTOT}} \quad (17)$$

It results that the maximum differential error will be about 15% of the maximum offset of the operational amplifier of the second stage 54. There is another advantage, not obvious either. If one takes a closer look at the final expression (17) of the differential error:

$$\Delta_{\text{err}} = \underbrace{\left| 1 - \frac{Gm_p}{Gm_n} \right|}_{\text{MOBILITY}} \underbrace{V_{\text{offTOT}}}_{\text{OFFSET}} \quad (18)$$

The expression (18) is composed of two factors, one dependent mainly on the mobility, the other on the random offset, hence mostly on impurities present on the surface and inside the oxide of the transistors of the two transistor doublets. These two factors are statistically independent from each other, hence the occurrence of the error is the product of the probability of the single event.

With a practical example it quite easy to explain this. One has seen that

$$0.86 \leq \frac{Gm_p}{Gm_n} \leq 1.16 \quad (19)$$

Based on the hypothesis that the maximum total offset is $V_{\text{offTOT}} = 30\text{mV}$, and that the values given are 4σ values, the maximum differential error will be:

$$\Delta_{\text{err}} = \pm 0.15 \cdot 30 = \pm 4.5\text{mV} \quad (20)$$

Because the two factors are independent from each other, the occurrence of this event will be the product of the probability, hence it is an 8σ value. This contributes to increase the yield of an input stage that is present many times in current and future ICs.

From the above equations one can derive that the differential error of a system in accordance with the present invention, as expressed in equation (18), is remarkably smaller than the maximum differential error of a prior art system, as expressed in equation (7).

Another embodiment is depicted in Fig. 6. In this figure, an apparatus is shown that comprises a folded cascode rail-to-rail input stage 61 and a second stage 64, comprising a rail-to-rail output stage amplifier. For a complete description of the output stage amplifier in Fig. 6, please refer to the following reference: "Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI", de Langen K.J. et al., Solid-State Circuits, IEEE Journal of, Vol. 29, Issue: 10 October 1998, pp. 1482 – 1496.

The input stage 61 comprises an NMOS transistor doublet N1, N2 with a first differential input 62.1, 63.1 for receiving input signals IN+, IN-. The input stage 61 furthermore comprises a PMOS transistor doublet P3, P4 with a second differential input 62.2, 63.2 for receiving input signals IN+, IN-. The transistors P7, P8, P9 and N11, N12, N13 complete the folded cascode input stage 61. The transistor pair P9, N13 acts as a voltage source that fixes the bias current in the folded branches (P7 to N11 and P8 to N12) and through P5 and P6 in the two transistor doublets P3, P4, and N1, N2. The second stage 64 is a class AB output stage composed by the transistors P10, N14, P16, and N15. The transistors P10 and N14 serve as voltage level shifter for biasing properly the gates of the two output transistors P16 and N15, in order to control their steady state bias current.

In order to be able to direct the analog input signals IN+, IN- either to the first transistor doublet N1, N2 or to the second doublet P3, P4, switching means are employed that selectively direct the analog input signal either to the first differential input 62.1, 63.1 or to the second differential input 62.2, 63.2. The switching function is controlled by a switching signal, preferably a digital switching signal, applied to the inputs 65.1, 65.2. In the present example, the switching signal has two states, either Φ or $\bar{\Phi}$. The switching means comprise eight switches S1 through S8. The switches S1 through S8 may be realized by transistors. The switches S1, S3, S5 and S7 close if the

switching signal Φ is applied while the switches S2, S4, S6 and S8 remain open. If the signal $\bar{\Phi}$ is applied to the switches S2, S4, S6 and S8, these switches are closed and the switches S1, S3, S5 and S7 are open. That is, if Φ is active, the PMOS transistor doublet P3, P4 processes the input signals IN+ and IN-. At the same time, the NMOS transistor doublet N1, N2 remains active since the first differential inputs 63.1, 62.1 are connected to a reference voltage REF_HIGH, that is made available at a node 66.1. If $\bar{\Phi}$ is active, the NMOS transistor doublet N1, N2 process the input signals IN+ and IN-. At the same time, the PMOS transistor doublet P3, P4 remain active since the second differential inputs 63.2, 62.2 are connected to a reference voltage REF_LOW. The reference voltage REF_LOW is made available at a node 66.2.

The positive supply rail may be V_{DD} , for example, and the negative supply rail may be V_{SS} , for example. The output OUT of the apparatus is connected via a feedback loop 68 and switches S1 and S2 back to the negative differential input terminals 61.2, 62.2, depending on the phase Φ and $\bar{\Phi}$.

The apparatus 70 of Fig. 6 can be simplified, as illustrated in Fig. 7. It comprises a differential input IN+, IN- and an output OUT. There is a feedback loop 68 between the output OUT and the negative input IN-. The input stage 61 is depicted as rectangular box inside the amplifier 64. Also visible in this Figure are the phase inputs 65.1, 65.2. The control signal applied to these phase inputs 65.1, 65.2 control the operation of the transistors doublets of the input stage 61.

Part of a source driver bank 80 with n apparatus 70 is schematically illustrated in Fig. 8. The differential input signals IN1+, IN2+, IN3+ through INn+ and IN1-, IN2-, IN3- through INn- are fed to the differential inputs of the n apparatus 70. The differential input signals are received via a bus 81. This bus 81 may be identical to the bus 43 in Fig. 4, for instance. These differential input signals are used to control the respective columns of an LCD screen. Each apparatus 70 comprises an amplifier 64, depicted as triangle, and an input stage 61, depicted as rectangular box inside the triangle. The input stage 61 has two transistor doublets, not visible in Fig. 8, which alternatively process the differential input signals. Control signals Φ and $\bar{\Phi}$ are applied to the respective terminals of the apparatus 70, as illustrated in Fig. 8. Depending on the state of these control signals, the differential input signals are either directed to an NMOS transistor doublet or to a PMOS transistor doublet of the input stage. In order to keep the idle transistor doublet

active, two reference voltages REF_HIGH and REF_LOW are provided via two supply lines 66.1, 66.2 to the input stages 61.

An apparatus in accordance with the present invention may comprise a control signal generator 90, as illustrated in Fig. 9. The control signal generator 90 receives data via a bus 91. The data are sent by a display controller, for example. The bus 91 may be identical to the bus 43 in Fig. 4. The apparatus 90 comprises a logic circuitry to generate the two phase signals Φ and $\bar{\Phi}$. These phase signals are fed to the n apparatus 70.

As explained above, and as can be derived from the Figures, the invention provides for an apparatus where none of the transistor doublets of the input stage are allowed to switch off. While the differential input signal is being processed by one of the two transistor doublets, the other transistor doublet, referred to as idle transistor doublet, is kept active. The idle transistor doublet is temporarily connected to the respective reference voltage (either HIGH_REF or LOW_REF) and the other transistor doublet is temporarily connected to the differential input.

The present invention allows to provide a constant offset over the whole input/output range. An apparatus, according to the present invention, provides a high precision differential voltage.

An apparatus, according to the present invention, is well suited for being used in thin film transistor liquid crystal display (TFT-LCD) source drivers, for example, since these drivers require a high precision differential voltage in order to drive the flat display to avoid visual defects or artifacts.

The inventive circuitry is well suited for use in source driver for display applications with present (VGA and UXGA) and future resolutions.

It is appreciated that various features of the invention which are, for clarity, described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment may also be provided separately or in any suitable subcombination.

In the drawings and specification there has been set forth preferred embodiments of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.

CLAIMS

1. Apparatus (80) comprising an input stage (50; 61) with
 - an NMOS transistor doublet (N1, N2) having a first differential input (52.1, 53.1; 62.1, 63.1) for receiving input signals,
 - a PMOS transistor doublet (P3, P4) having a second differential input (52.2, 53.2; 62.2, 63.2) for receiving input signals, and
 - switching means for receiving and selectively directing analog input signals either to said first differential input (52.1, 53.1; 62.1, 63.1) or to said second differential input (52.2, 53.2; 62.2, 63.2), said means being controlled by a switching signal (Φ , $\bar{\Phi}$), whereby the ratio of the transconductance of the NMOS transistor doublet (N1, N2) and the transconductance of the PMOS transistor doublet (P3, P4) is kept constant.
2. The apparatus (80) of claim 1, wherein the switching means direct the input signals to said first differential input (52.1, 53.1; 62.1, 63.1) if the input signals have positive gamma data and to said second differential input (52.2, 53.2; 62.2, 63.2) if the input signals have negative gamma data.
3. The apparatus of claim 1 or 2, wherein
 - the NMOS transistor doublet (N1, N2) comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node (IN+) and the gate of the second of the two NMOS transistors is connectable to a second input node (IN-),
 - the PMOS transistor doublet (P3, P4) comprises two PMOS transistors, each having a gate, whereby the gate of the first of the two PMOS transistors is connectable to the first input node (IN+) and the gate of the second of the two PMOS transistors is connectable to the second input node (IN-).
4. The apparatus of claim 3, wherein
 - the gate of the first of the two NMOS transistors is connectable to a first reference node (66.1) being biased with a first reference voltage (HIGH_REF), and the gate of the second of the two NMOS transistors is connectable to the first reference node (66.1) being biased with a second reference voltage (LOW_HIGH),

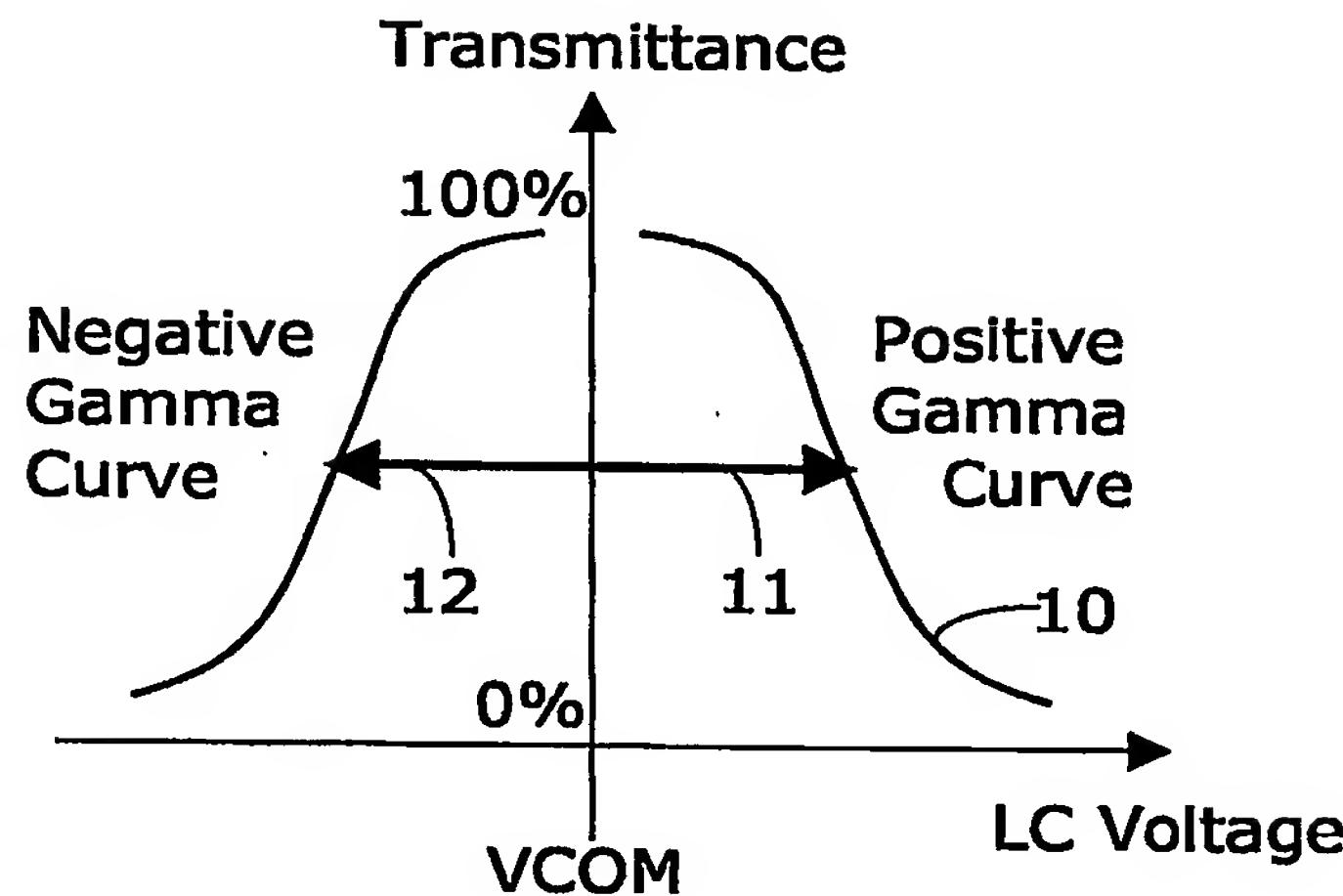
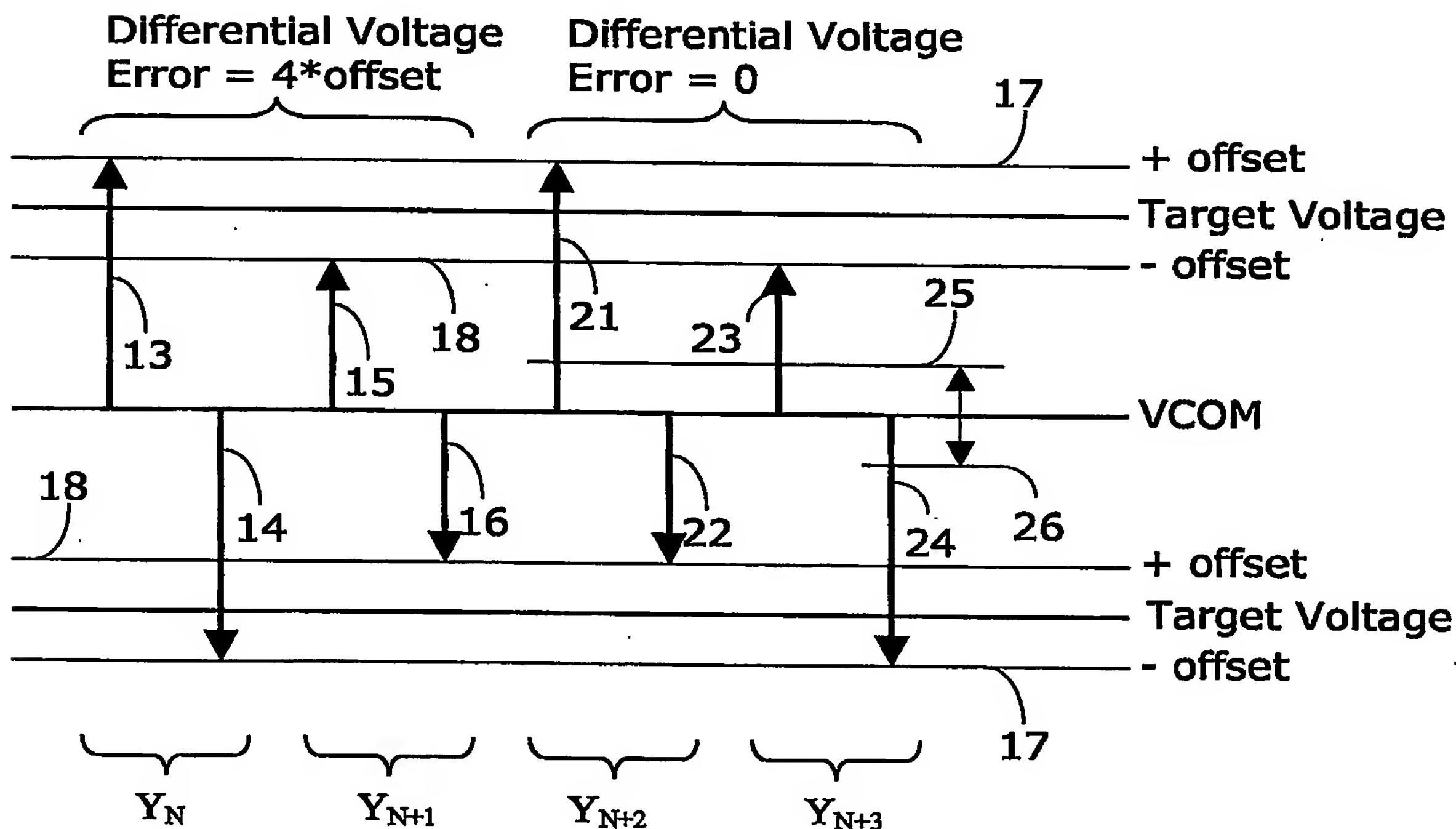
- the gate of the first of the two PMOS transistors is connectable to a second reference node (66.2) being biased with a second reference voltage (HIGH_LOW) and the gate of the second of the two PMOS transistors is connectable to the second reference node (66.2).
5. The apparatus of claim 1, wherein the input stage (50; 61) is a rail-to-rail input stage.
 6. The apparatus of claim 1, wherein the switching means comprise a plurality of switches (S1 through S8) in order to selectively direct the input signals to said first differential input (52.1, 53.1; 62.1, 63.1) or said second differential input (52.2, 53.2; 62.2, 63.2).
 7. The apparatus of claim 1 or 2, wherein said switching signal (Φ , $\bar{\Phi}$) is a digital switching signal.
 8. The apparatus according to one of the claim 1 through 4, wherein transistors serve as switches (S1 through S8).
 9. The apparatus of claim 1 or 2, wherein the NMOS transistor doublet (N1, N2) and the PMOS transistor doublet (P3, P4) are part of a folded cascode rail-to-rail input stage (61) and wherein the folded cascode rail-to-rail input stage (61) is connected to a second stage (64) comprising a rail-to-rail output stage amplifier.
 10. Apparatus comprising a source driver bank (80) with a plurality of apparatus according to one of the previous claims, and further comprising a bus (43; 91) for receiving input signals.
 11. The apparatus of claim 10, further comprising a gate driver bank (45) and an LCD panel (46).
 12. The apparatus of claim 10 or 11, further comprising a control signal generator (90) for generating the switching signal (Φ , $\bar{\Phi}$).
 13. The apparatus of claim 10, 11 or 12 being part of a panel module (40).

ABSTRACT

Operational amplifier with constant offset and apparatus comprising such an operational amplifier

Apparatus (80) comprising an input stage (61) with an NMOS transistor doublet having a first differential input for receiving input signals, and a PMOS transistor doublet having a second differential input for receiving input signals. The apparatus (80) further comprises switching means for receiving and selectively directing analog input signals either to the first differential input or to the second differential input. The means are controlled by a switching signal (Φ , $\bar{\Phi}$) in a manner to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant.

(Fig. 8)

**Fig. 1****Fig. 2**

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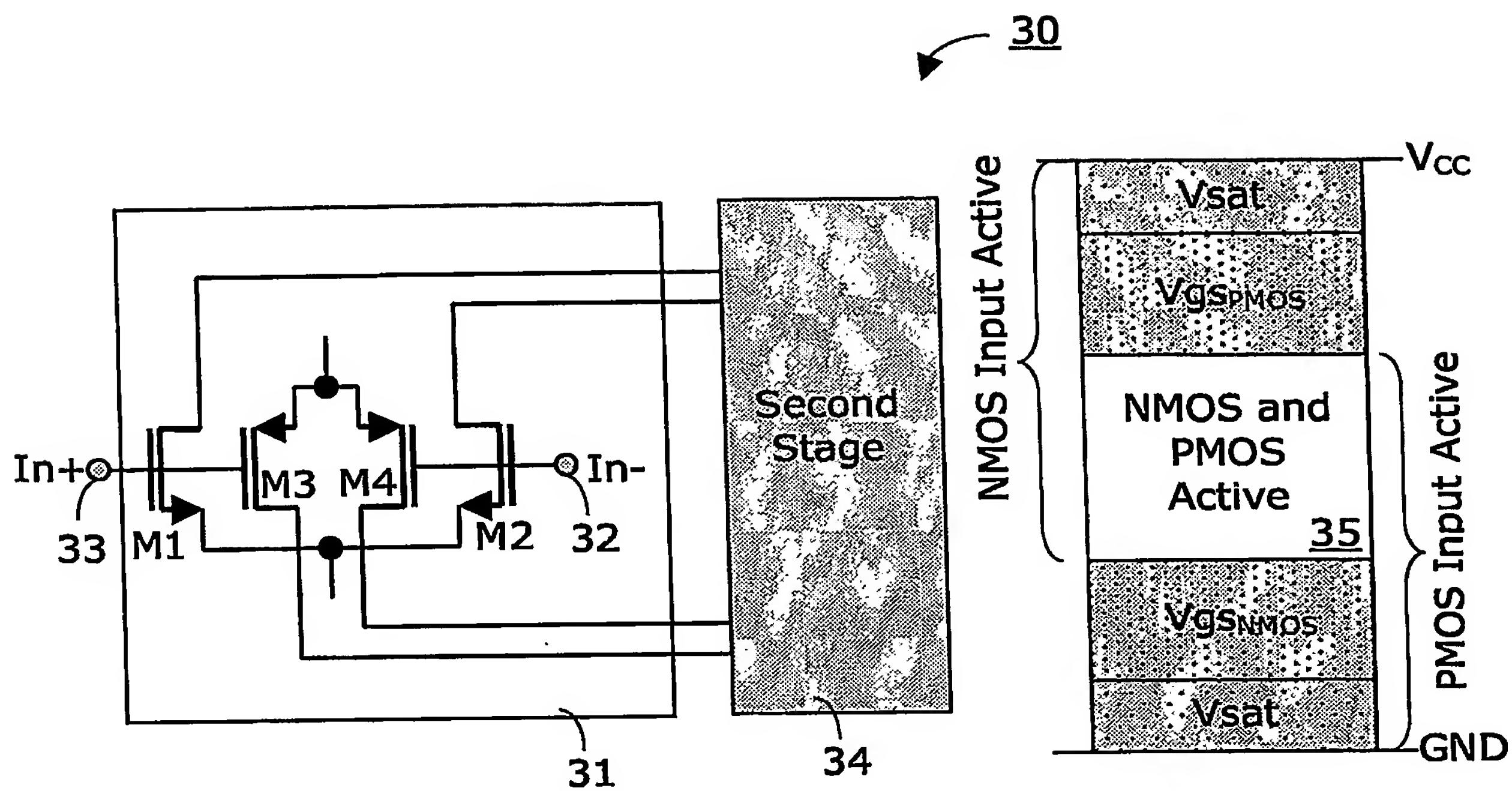


Fig. 3

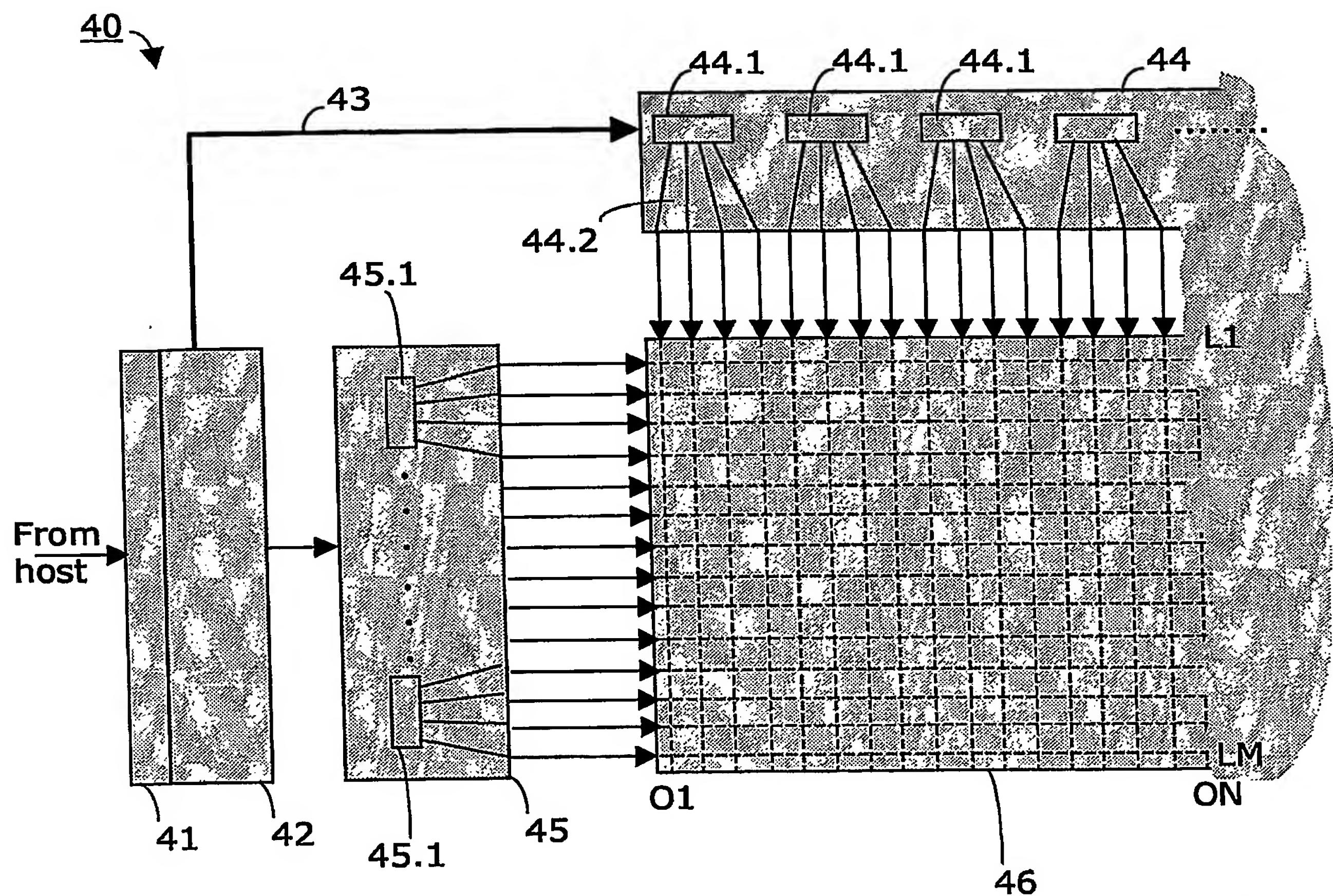
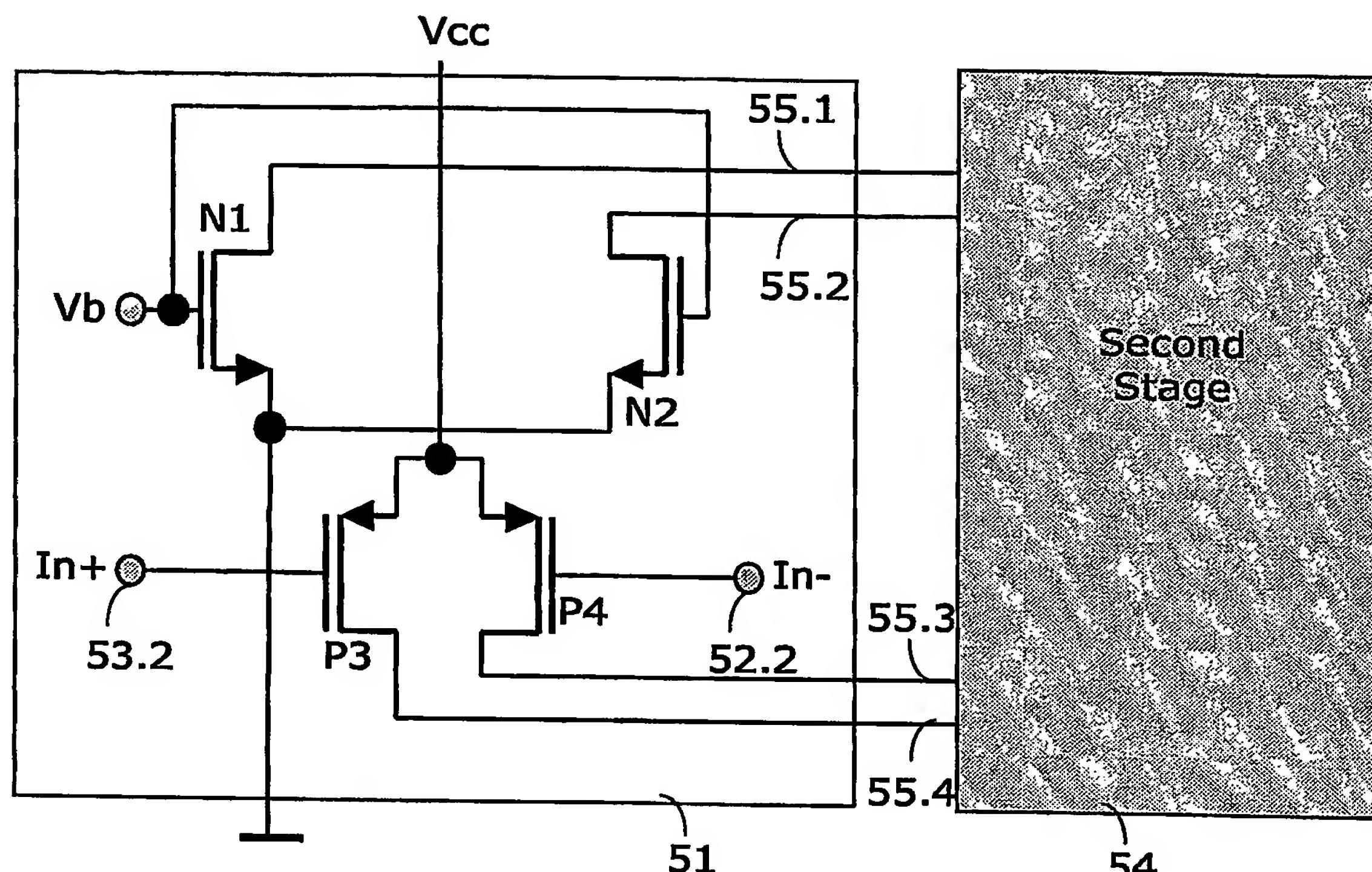


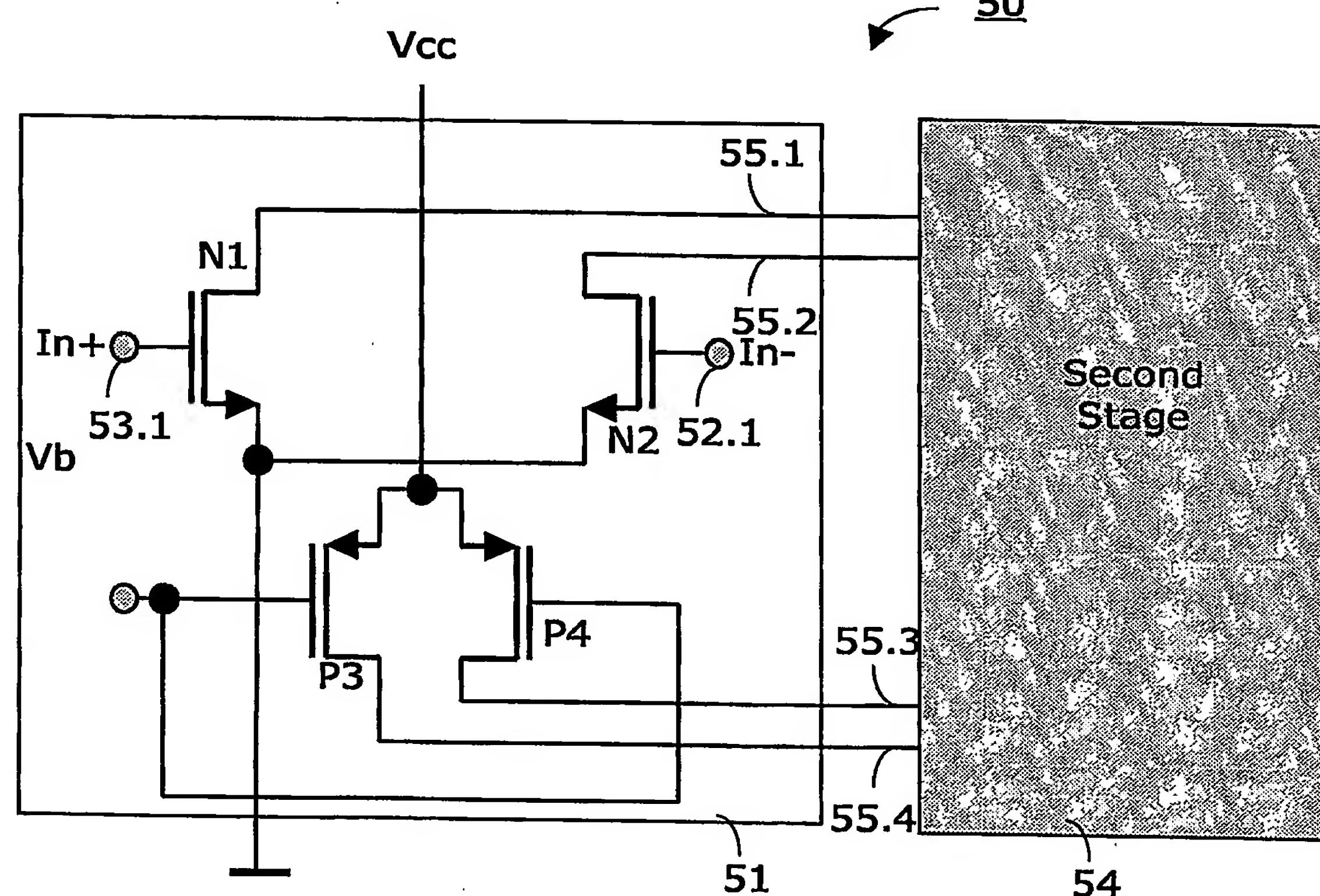
Fig. 4

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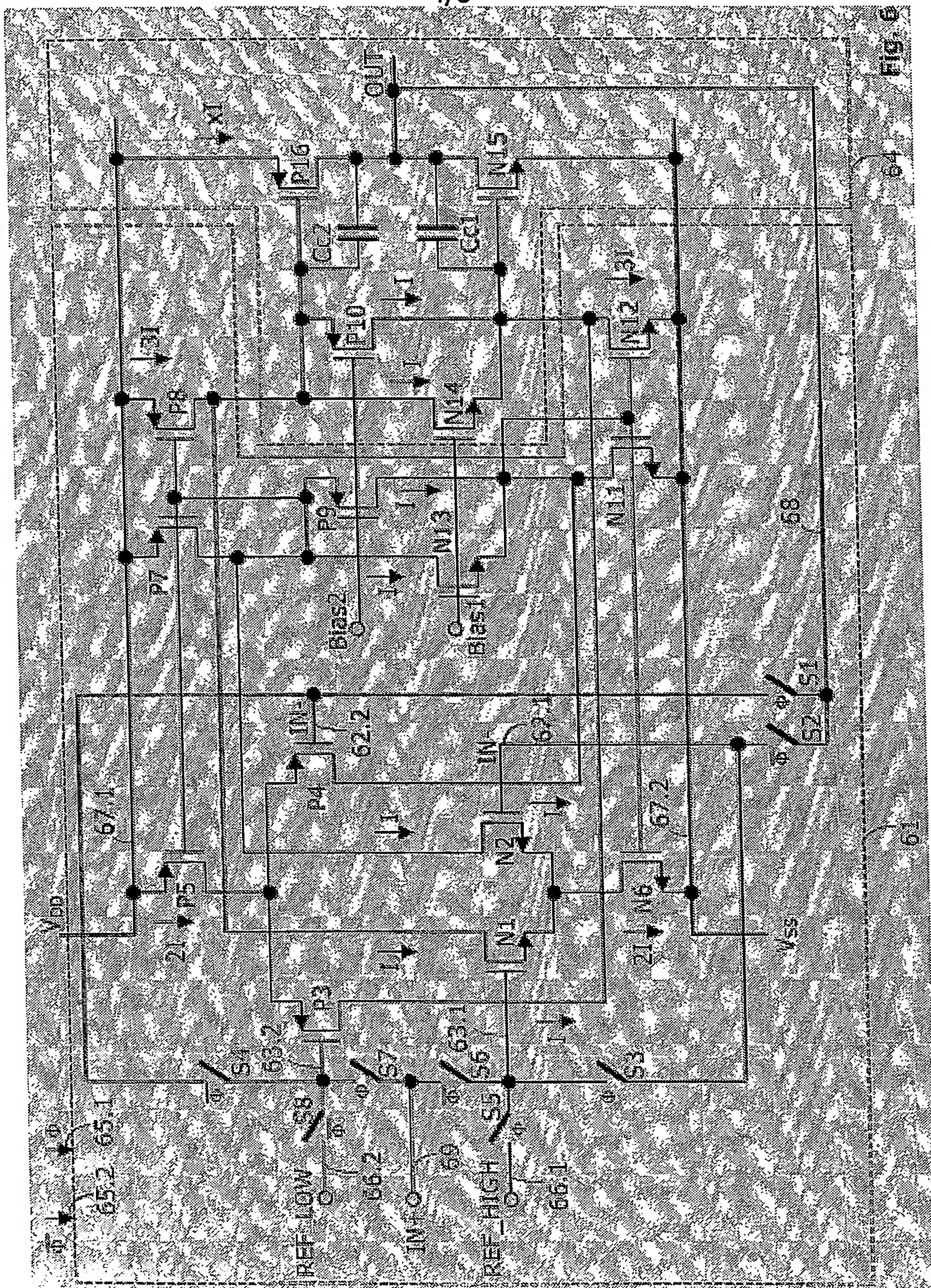
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**Fig. 5A**

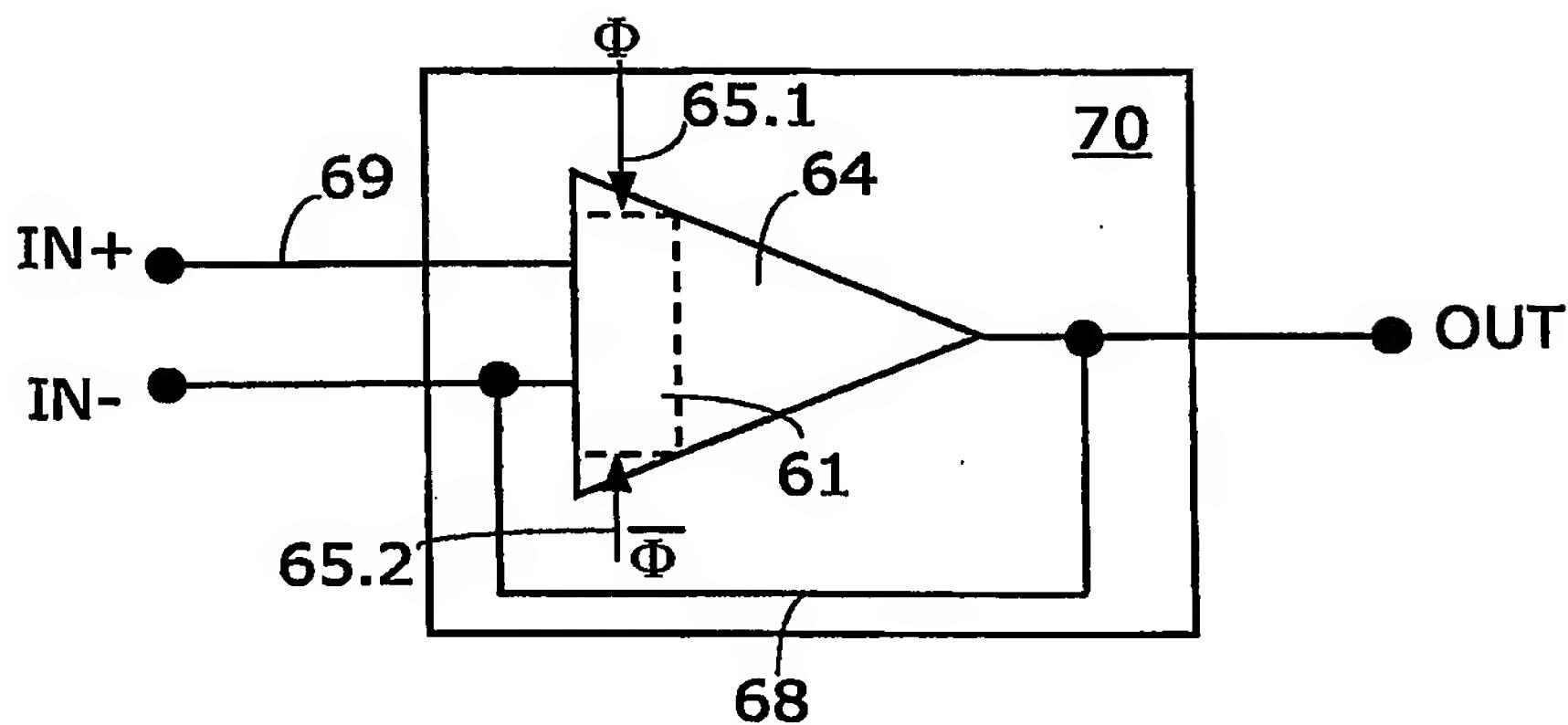
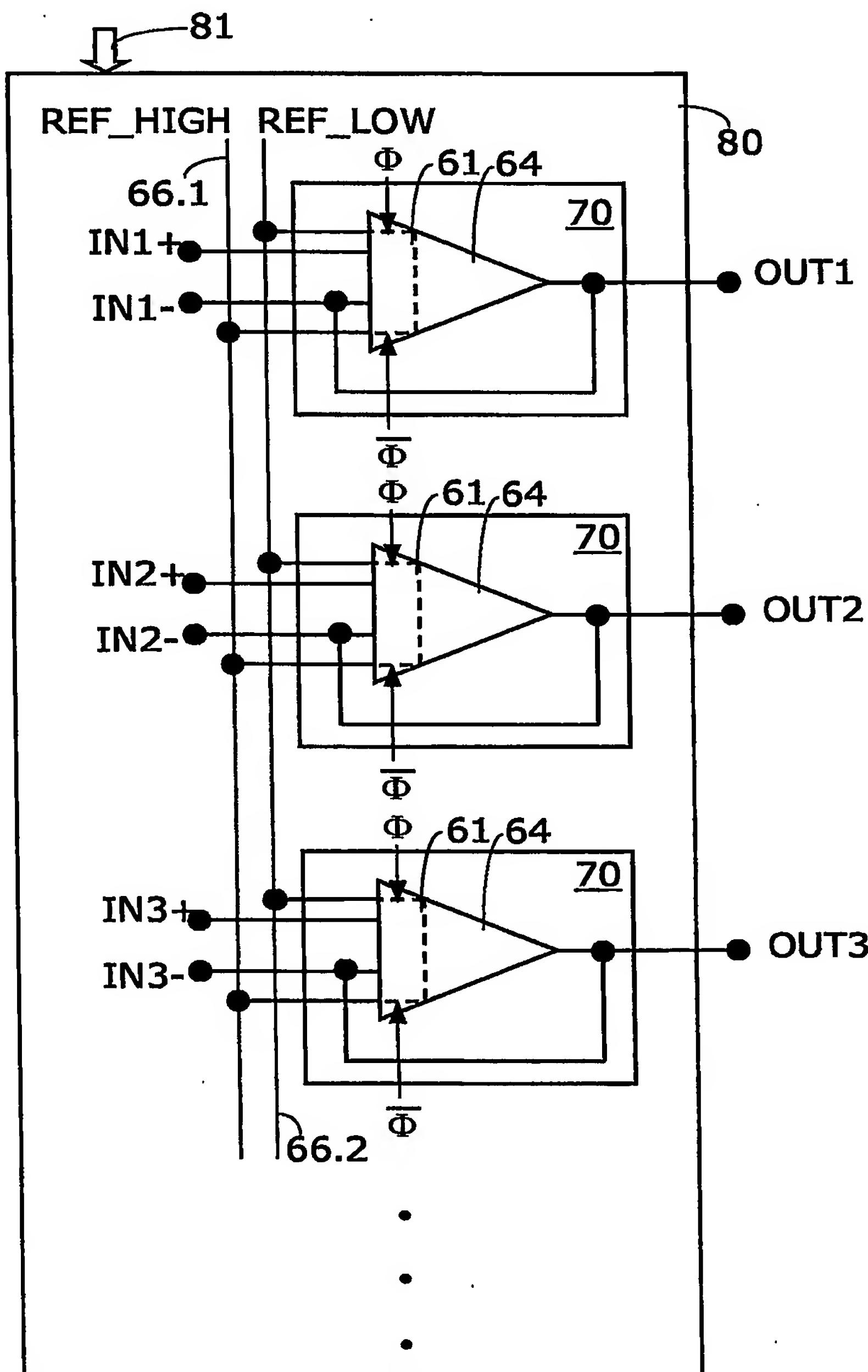
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**Fig. 5B**

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**Fig. 7****Fig. 8**

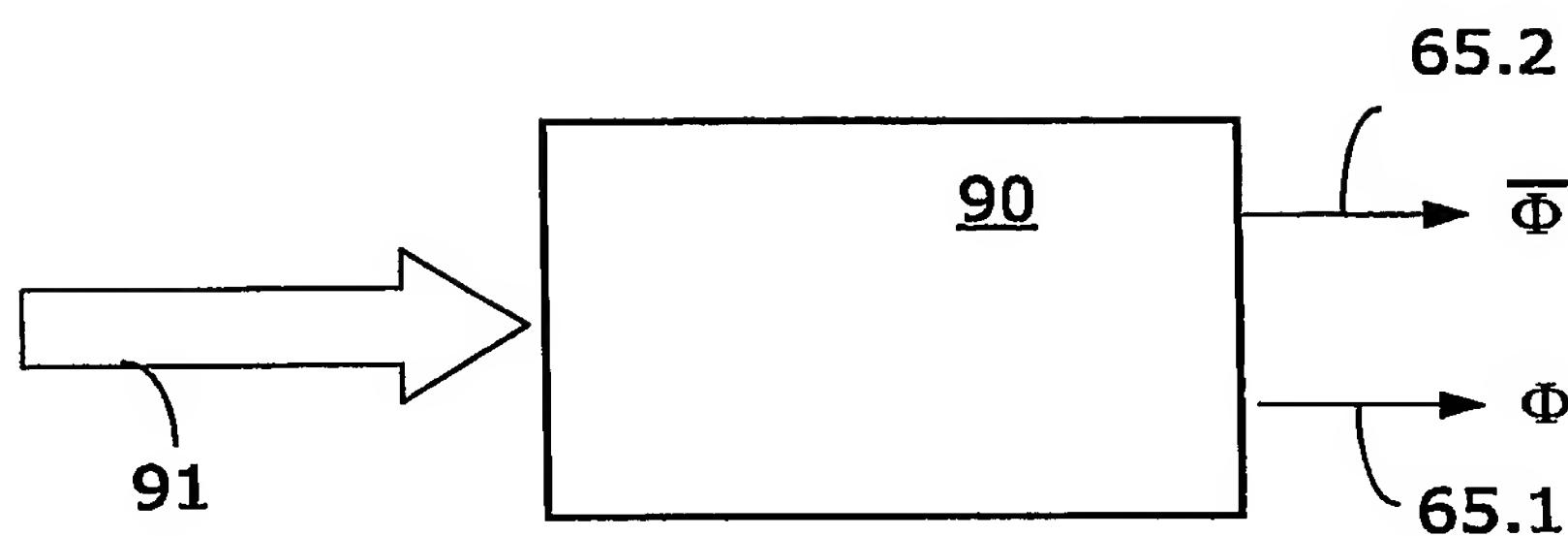


Fig. 9

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